Transistor-Level Transient Modelling of Thermal Transport in Electronic Devices
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Proper thermal transport modelling in an electronic device requires developing a hierarchical multi-scale model. The hierarchical methodology incorporates physics-based models at different length scales ranging from nanometers to a few millimetres. Appropriate modelling techniques for each level of the hierarchy are developed. Different levels of the hierarchy include atomistic-level (a few tens of nanometres), to transistor and logic-gate level (a few microns), to functional blocks level (a few hundreds of micrometres), and finally to the package level (a few millimetres). Simulations start at the smallest length scale (atomistic level), and information transfer to the next higher length level is through the definition of a compact model or an effective physical property.

The first step of this hierarchical modelling is to simulate thermal transport in thin films and nanowires using atomistic-level techniques. Our group has done extensive work on this part of project and have developed atomistic-level techniques for thermal transport modelling in such systems. The results of the atomistic-level simulations are then transferred to the next level in the hierarchy of length scales (i.e., transistor and logic gate level) in the form of effective thermal conductivity and thermal diffusivity for different parts of the transistor.

The MEng student will work on the transistor and logic-gate level modelling, continuing our group's work in 3D models of different basic logic gates based on FinFET and MOSFET technologies, performing transient simulations. A parametric study of the effect of geometrical parameters of the FinFET and MOSFET technologies on the predicted equivalent thermal conductivity will also be performed.

Research area: Nano-Heat Transfer