CMC/SCM

Introduction to
Micragem:
A Silicon-on-Insulator Based Micromachining Process

Report ICI-138
V3.0 (Beta version)

December 14, 2004

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Revision History

REVISION	ACTIVITY	DATE
1.0	Document released and posted to http://www.cmc.ca/about/program/beams.html	November 27, 2003
2.0	Document updated with Design rules	December 19, 2003
3.0	Document reviewed after first test run and released for beta testing to 2nd test run designers	December 14, 2004

Table of Contents

1 Introduction

This document presents a high-level overview of the Micragem (Micralyne Generalized MEMS) prototyping technology, a brief description of design parameters, and a description of design rules. Figures of MEMS devices fabricated by Micralyne are included to demonstrate the process.

1.1. Intended Audience

This release is intended for graduate students and professors—particularly those involved in MEMS design—who have registered with CMC. To find out how to register, visit CMC's web site at:
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1.3. About Micragem

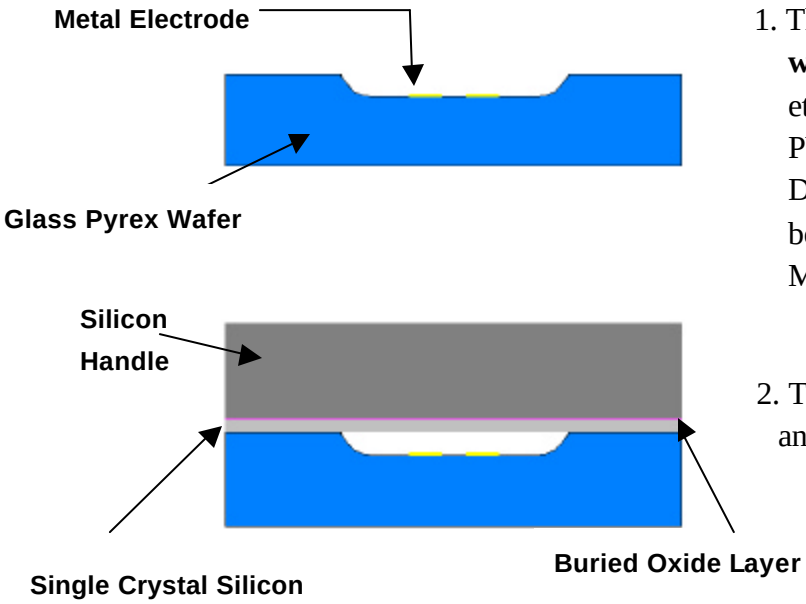
Micragem (Micralyne Generalized MEMS) is a Micro-Electro-Mechanical Systems (MEMS) prototyping process under development at Micralyne Inc. in conjunction with the Canadian Microelectronics Corporation. This technology differs from traditional MEMS processes by the materials used in the process, and by its variable geometry. Using Micragem, designers are able to vary the gaps between the structural layers thus adding more functionality to their designs.

This process enables users to develop fully suspended MEMS devices with metal electrodes (rather than silicon). Users of the process can select two gap depths (or combination of the two) during each run, as described below. This makes the Micragem process more versatile and flexible than other MEMS prototyping technologies, enabling designers to develop MEMS devices with gap sizes between layers. General specifics of the run are outlined below:

- A 10µm thick, single crystal silicon membrane over a 2µm, 10µm or combined 12µm gap.
- Each design is allocated a run space of 9mmx5mm or 4mmx5mm and designers receive a minimum of 15 Micragem chips for their submitted designs.

1.4. Overview of the Micragem Process

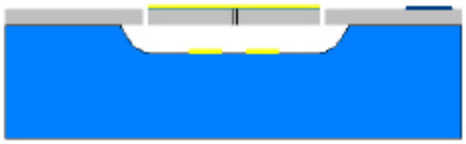
Figure 1-1 illustrates the high-level steps of how a device is fabricated using the Micragem prototyping process. A more detailed process description is given below.



1. The process begins with a **Pyrex wafer**. Cavities of two depths are etched in the Pyrex (MASK 1 PYREX – Shallow; MASK 2 - Deep). M**etal electrodes**, lines and bond pads are patterned (MASK 3 METAL1).

2. The SOI wafer (device layer down) is anodically bonded to the Pyrex.

3. The **silicon handle** wafer and **buried oxide layer** are etched away.



4. Low-stress metal is deposited. METAL2 and etch (DRIE) are lithographically patterned to release silicon microstructures.

Figure 1-1: Steps in the Micragem Prototyping Process

The following provides further details of the process illustrated in Figure 1-1:

1a) A 525 µm thick 7740 Pyrex bonding wafer is patterned with MASK 1 (PYREX - Shallow) and etched to the specified depth of 2µm (±0.2µm).

1b) Second mask, MASK 2 (PYREX – Deep) is patterned to the specified depth of 10µm (±0.3µm).

NOTE: This etch defines the depth in Pyrex and can be used to create cavities, gaps, microfluidic channels, grooves for electrode lines, and so on. Designer can also use both masks concurrently to define depths of 12µm.

1c) METAL1 is patterned using lift-off technique so that the substrate is lithographically patterned with MASK 3 (METAL1). This layer consists of 50nm titanium, 50nm platinum, and 200nm gold. This mask is used to define base/ground electrodes, metal lines, and bonding pads.

NOTE: METAL1 can appear within the PYREX etch or on the surface of the Pyrex. This is usually used for METAL1 to METAL2 connections through the silicon or to fully enclose a cavity and still have an access to the metal within the cavity. This will be further outlined in section 3.6.

2) Following METAL1 patterning, an SOI wafer is anodically bonded, device side down, to the patterned side of the Pyrex wafer. No bond alignment is required, thus no compensation in design is required between the membrane and the bottom metal. The SOI wafer consists of a 525 µm single crystal silicon "handle" and a single crystal "device" layer with a sufficiently thick buried oxide separating them.

3) The handle and buried oxide portions of the wafer are **completely** etched away in a wet process, leaving the single crystal silicon membrane (device layer) over the cavities/gaps. The thickness of this layer is (10µm). Note that no features are patterned to the bottom side of this layer.

4a) Chrome/gold (METAL2) layer is deposited on the silicon surface, and lithographically patterned with MASK 4. This layer consists of 100Å thick chrome and 750Å thick gold. METAL2 is then etched to expose the silicon using a wet etch process. This metal layer is mainly used for top electrodes and reflective surfaces (for micromirrors or for optically testing a RF switch or resonator). This is also a useful layer for labeling devices.

4b) The last lithography/etch step is with MASK 5 (SCSi). Final structures are patterned with a photoresist mask and released in a plasma etch. Finally, the wafer is diced and the final devices are revealed.

Important: *In the second test run of Micragem process in Winter 2004, closed ended microfluidic channel with METAL1 electrodes accessible externally can now be developed.*

2 Designing with Micragem

In this chapter, we will describe the technology file for Micragem process and some useful information on how to use the technology file for the designs.

2.1. Technology File Description

The technology file to design devices with Micragem technology is being developed by Micralyne and CMC in L-Edit (V8.2, 9.2) or MEMSPro V4.0 and Cadence formats. This file will be supplied in TDB format to selected users of the Micragem process. The following table explains various layers used in this technology file:

Layer Name	CIF #	GDSII #	Description
INFO (Die Size)	CPG	46	This layer outlines the die size and active design space.
PYREX Etch - Shallow	PYS	42	This layer is used to represent bulk-etched micro features (gap definition, channels, chambers, etc.) in the glass substrate to a depth of 2µm. (
PYREX Etch - Deep	PYD	43	This layer is used to represent bulk-etched micro features (gap definition, channels, chambers, etc.) in the glass substrate to a depth of 10µm. Designer can use these two layers (Pyrex Etch-Shallow & Deep) concurrently to define the depth of 12 µm
METAL1 (on Glass)	MET	49	This layer is to represent where metal lines/traces and pads will be placed in the Pyrex cavity
SCSi	DRI	51	This layer represents the remaining/released Single Crystal Silicon after the final deep reactive ion etching (DRIE).
Hole_SCSi	HSI	52	This layer is used to generate holes in SCSi layer
METAL2 (on Silicon)	LSG	56	This layer shows the upper metal lines/traces, pads, and reflective surfaces.
Hole_M2	HME	57	This layer is used to generate holes in METAL2 (on Silicon) layer
3-D fill			This layer is not used in 2-D layout and is only used to define the cavity in glass substrate when extracting the third dimension of the model for simulation purposes.

Table 2.1: Description of design layer of Micragem process

2.2. Important Design Considerations

The following illustrations demonstrate the process of laying out a simple design while keeping to the design rules described in Section 3. Figures 2-1 and 2-2 show the side and top views of the cantilever beam used in the example. Figure 2-3 shows the scanning electronic microscope (SEM) images of the final device.

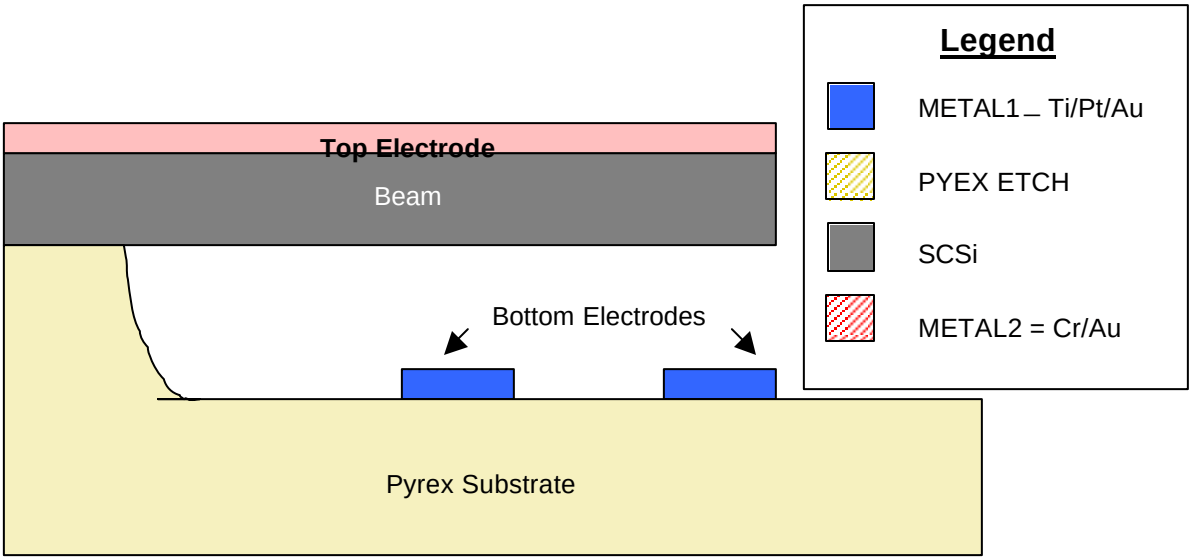


Figure 2-1: Side View of Cantilever Beam Designed with Micragem

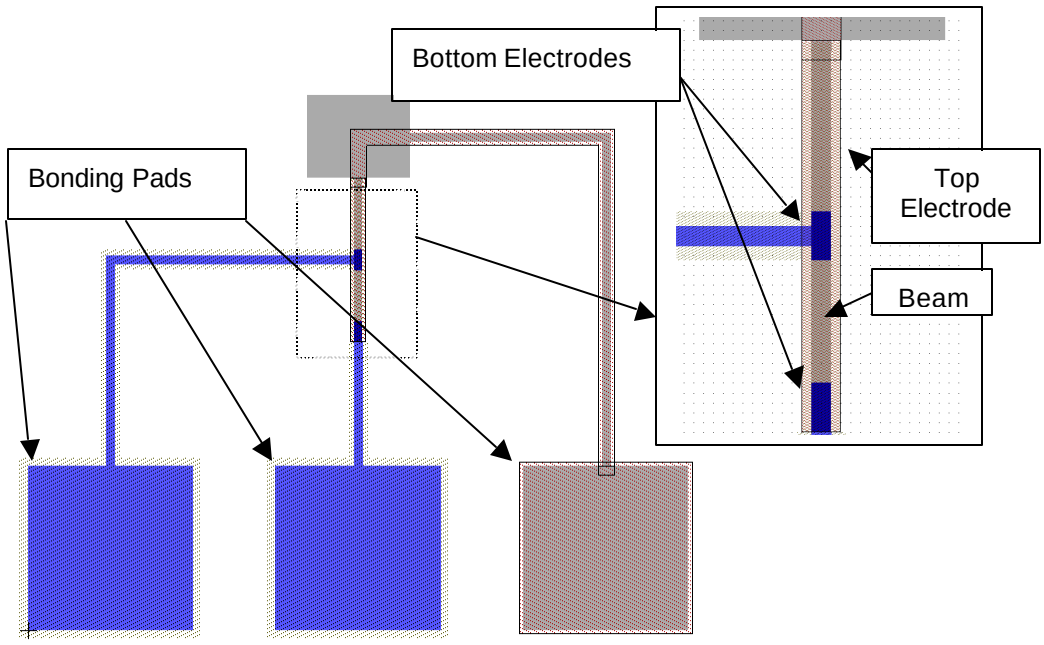


Figure 2-2: Top View (L-Edit Layout) of Cantilever Beam Designed with Micragem

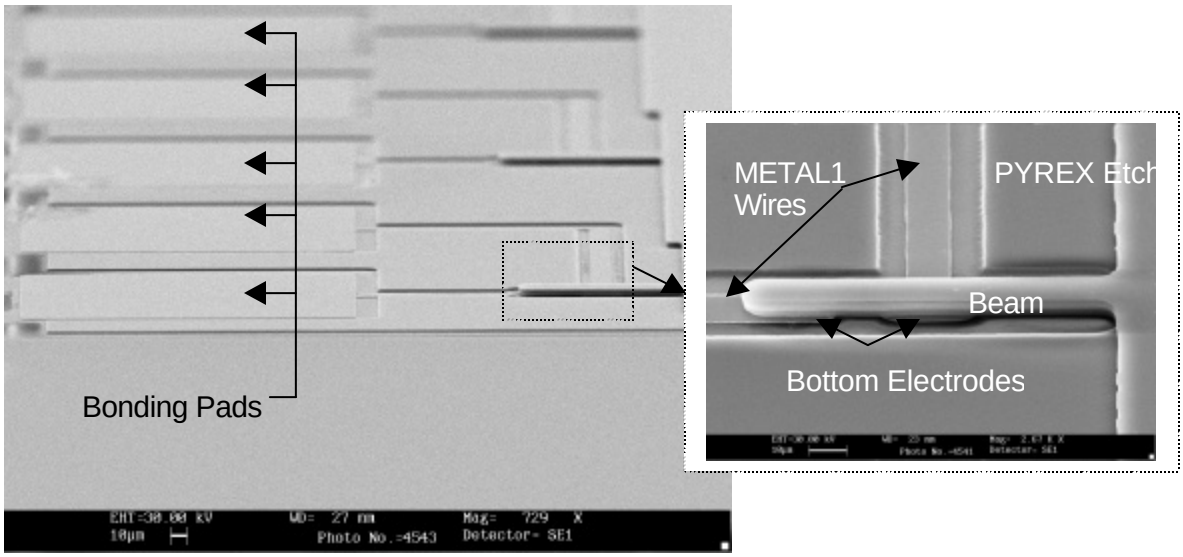


Figure 2-3: SEM Images of Final Cantilever Device Designed with Micragem

The technology file is first opened with the layout shown in Figure 2-4. The green, rectangular box represents the designers' working area. **Design features must stay within this box.**

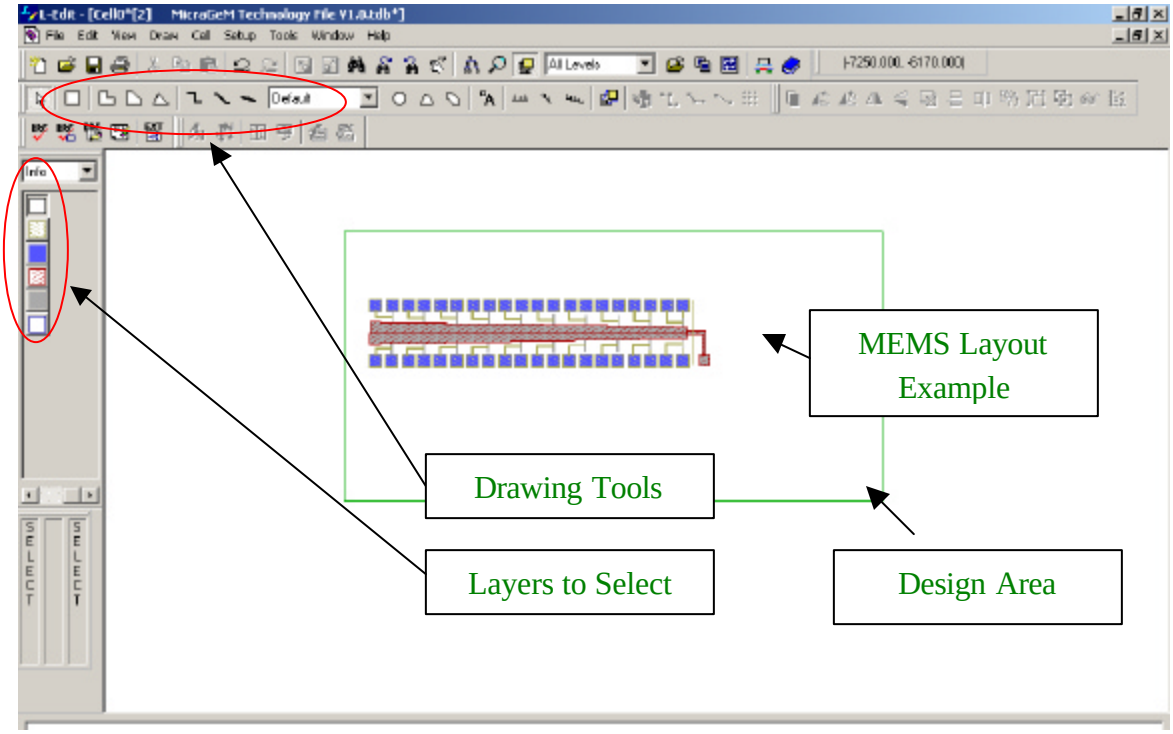


Figure 2-4: Micragem Technology File

Because multiple layers will appear on top of each other, two of the layers have been created with a transparent hatched pattern (see the PYREX Etch - Shallow and METAL2 layers in Figure 2-5). This allows designers to see the outline of multiple layers at once without having to turn layers on and off. Refer to Figure 2-5 for examples and explanation of these layers.

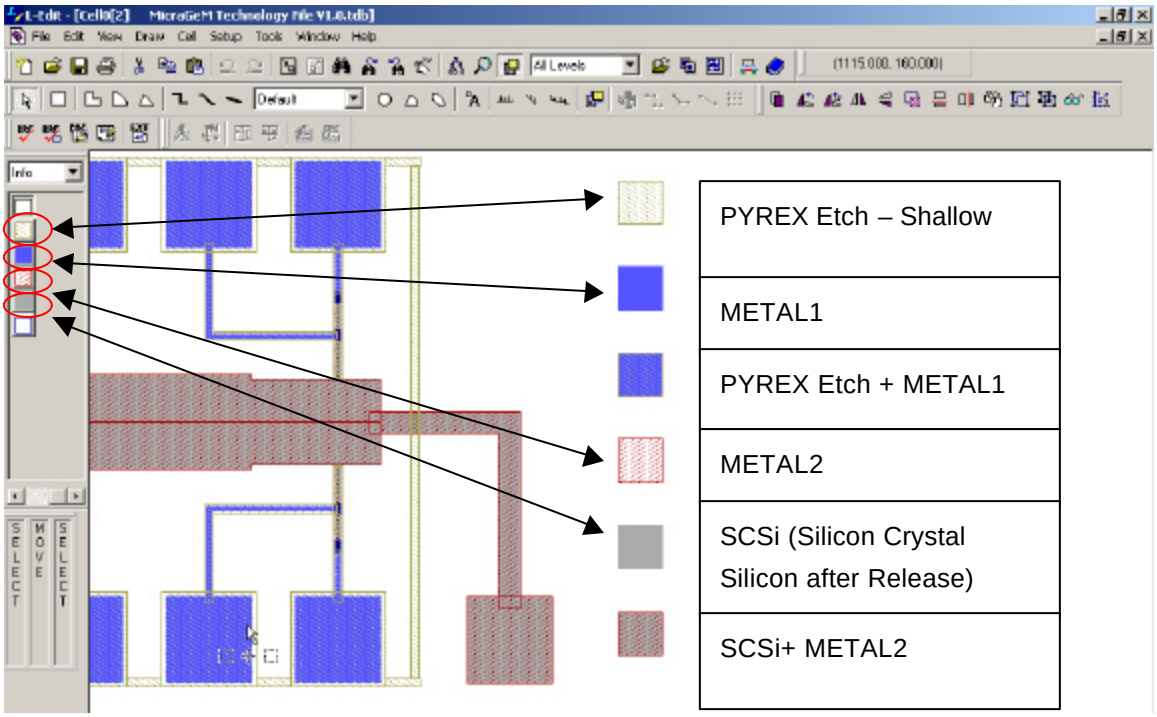


Figure 2-5: Layers in the Micragem Technology File

NOTE: PYREX Etch – Deep is not shown because of the simplicity of the example but will be included in the technology file.

2.3. Additional General Design Considerations

The additional, more general comments below will be helpful in ensuring that the design conforms to process requirements and can be manufactured without error:

1. Technology files and the user guide of Micragem can be downloaded at: http://www.cmc.ca/about/program/beams.html
2. In technology file, you will find two green boxes with layer *info (die size)* layer in the cell entitled *die outline* as shown in figure 2-6. These boxes represent the two die-size (9mm × 5mm, 5mm × 4mm) which Micralyne offers for Micragem process. Use the size of this box for which you have been allocated the space from CMC and delete the other box.

3. While using the MEMS-Pro technology file be sure **not to modify** green rectangular box that you are using. This cell is intended to act as design guide, and modifying this cell is likely to result in designs being misplaced/misaligned at the wafer level.
4. When drawing a long, thin wire in the MEMSPro design tool, use a wire object instead of a freeform polygon tool. This will greatly reduce the chance of having erroneous width irregularities (e.g. zero width). It's also much faster to draw. When using such a tool, use butt ends and layout joins, or round ends and joins if the radius of curvature is 20 µm or greater. Rounded features are more difficult to manufacture, and an excessive number of such features may cause the design to be unsuitable for the Micragem process.

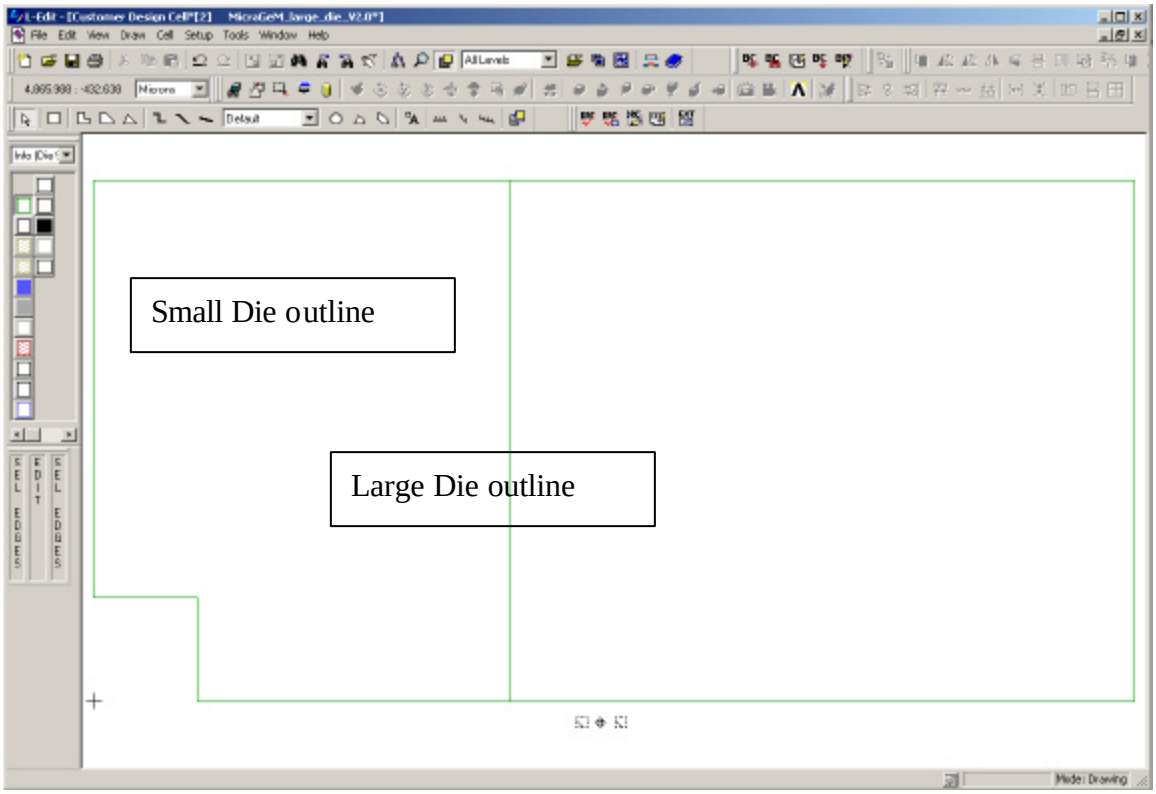


Figure 2-6: Two Layout Die Size Layers

3 Micragem Design Rules

This chapter describes the design rules users should follow in order to fabricate their designs using the Micragem process. The use of design rules ensures the highest rate of successful fabrication. The design rules for Micragem evolved through process development, the experience of Micralyne staff and from previous Micragem runs. These rules are dictated by the process constraints and individual process steps. The design rules are mandatory and violation of these rules may result in the design being rejected for submission.

The following sections describe these rules in detail. These rules are defined in the technology file (TDB file) provided on CMC's web site at:
http://www.cmc.ca/about/program/beams.html

3.1. Rule 1: Multi Pyrex Cavity Depths

Two masks are allocated to defining cavity depths. MASK 1 (Pyrex – Shallow) is etched to a 2µm ± 0.2µm depth. MASK 2 (Pyrex – Deep) is etched to a 10µm ± 0.3µm depth. However, these masks can also be used concurrently to form a 12µm depth. This is shown below in Figure 3-1.

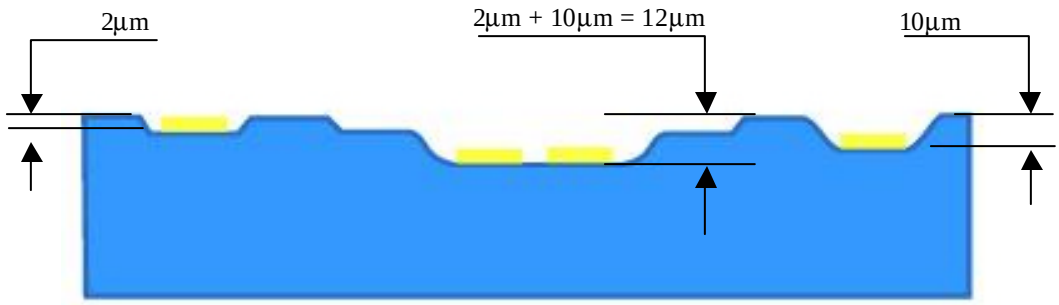


Figure 3-1: Multi Pyrex Cavity Depths

Take care in the layout of the masks if the combined depth is desired (12µm) because both etches are isotropic and alignment tolerance is ±2µm. Isotropic etch is explained below as part of Rule 1 – Minimum feature size of Pyrex.

3.2. Rule 2: Minimum Feature Size of PYREX Etch

- Sub-Rule 2(a): The minimum feature size for the PYREX Etch layer is to be no less than 5µm for MASK 1 (Pyrex – Shallow). However, if METAL1 is used in

this 2µm cavity, the minimum feature size for the PYREX etch layer is to be no less than 8µm for MASK 1 (Pyrex – Shallow).

- Sub-Rule 2(b): The minimum feature size for the DEEP PYREX Etch layer is to be no less than 10 µm

The PYREX Etch layer is an *isotropic* etch, which means that etch is not preferential in any direction. If the mask is patterned for an opening of *m* width and etched to a depth of *d*, the final width of the feature will be 1.2 times the depth on each side, plus the feature. This is shown below in Equation 3-1 and Figure 3-1 with the minimum m=5µm feature etched to a depth of d=10um, giving a final $W_{channel}$=29µm. (If the feature has a minimum m=5µm etched to a depth of d=2µm. This would give a minimum $W_{channel}$ = 9.8um.)

$$W_{channel} = m + 2(1.2d) = (10 + 2(1.2 \cdot 10))mm = 34mm \quad \text{(Equation 3-1)}$$

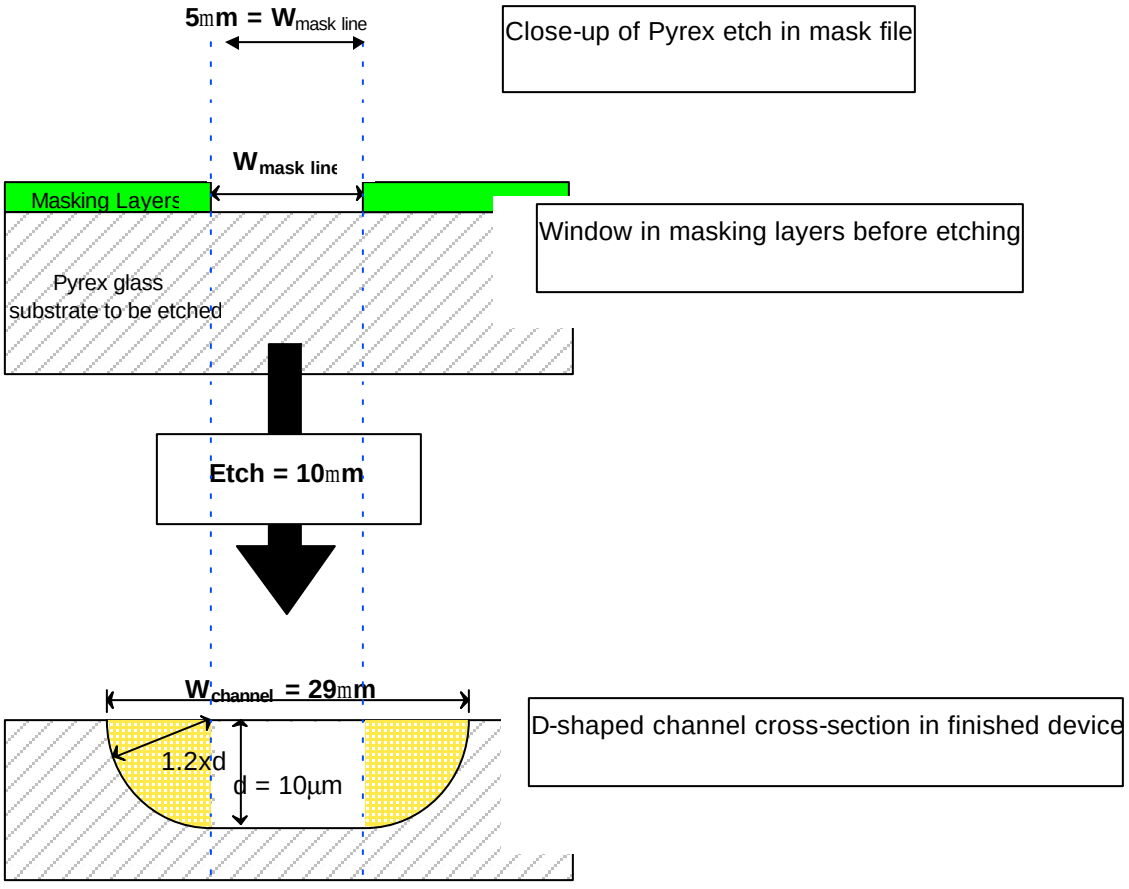


Figure 3-2: Appearance of Features Before and After Isotropic Etching

Note: If the designer requires METAL1 to be situated at the bottom of the Pyrex cavity (and not on any of the curved edges), the mask layout for the Pyrex etch should be at least the width of METAL1 feature PLUS 2µm all around to compensate for alignment tolerance (see Rule 6 for more details).

3.3. Rule 3: Pyrex features to be linked together

Designers must ensure that all features on both PYREX Etch layers are linked together with at least 5µm lines **unless fully enclosed features (such as microfluidic channels) are required.** An example is shown in Figure 3-3. This rule is not incorporated in the design rule-checking file of MEMSPro/Cadence

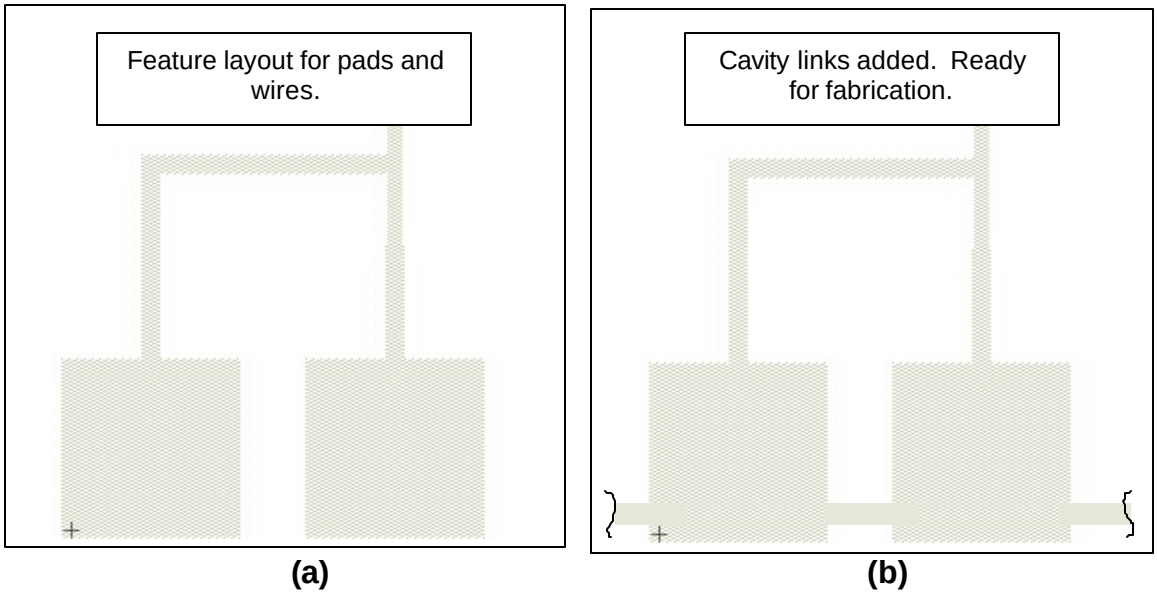


Figure 3-3: PYREX ETCH Layer
(a) Design Layout for Counter Sinking Wires and Electrode Pads
(b) Cavity Links Added to Design Layout

3.4. Rule 4: METAL1 (on Glass) Minimum Feature Size

- The minimum feature size for the METAL1 (on Pyrex) layer is to be no less than 10µm.

3.5. Rule 5 – Minimum Spacing Between METAL1 Layers

- The minimum spacing between features drawn for the METAL1 layer is to be no less than 10µm.

3.6. Rule 6: METAL1 Patterned

I**f the designer desires METAL 1 to be within the Pyrex etch** layer, the following requirements must be met:

- **Sub-Rule 6(a):** METAL1 must stay within, or stay lined up with ***DEEP PYREX Etch*** layer features in the mask design.
- **Sub-Rule 6(b):** METAL1 must be **at least** 2µm from the ***SHALLOW PYREX Etch*** PYREX ETCH layer features in the mask design.

Figure 3-5 shows the design layout defining the bottom electrodes, wires, pads, and gap definition for the cantilever beam example. All the wire traces and bonding pads are shown with the METAL1 layer enclosed in the PYREX Etch layer. Here the gap is defined by two PYREX Etch layers.

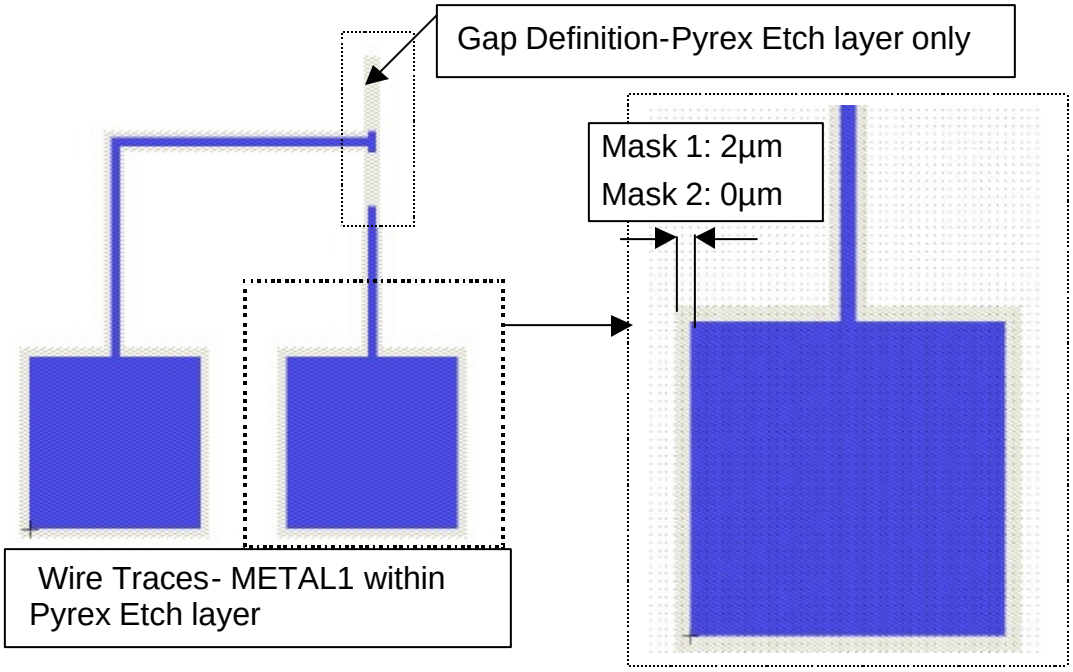


Figure 3-4: METAL1 Features Appear within Pyrex Etch Features

- **Sub-Rule 6(a): METAL1 to METAL2 connection through SCSi layer**

There are many advantages if METAL 1 can appear on the surface of the Pyrex. For example, a Metal 1 to Metal 2 connection can be formed through silicon via or a fully sealed microfluidics channel can have electrodes in the channel. **If the designer desires METAL 1 is to appear on the surface of the Pyrex**, the following requirements must be met.

- Metal on the Pyrex surface should have traces no wider than 10µm.
- Metal wider than 10µm must be within a Pyrex cavity. (See Figure 3-5 below).
- Surface Pyrex must be at least 10µm around surface METAL1. (This is an absolute minimum. The more surface Pyrex exposed, the better the bond.)

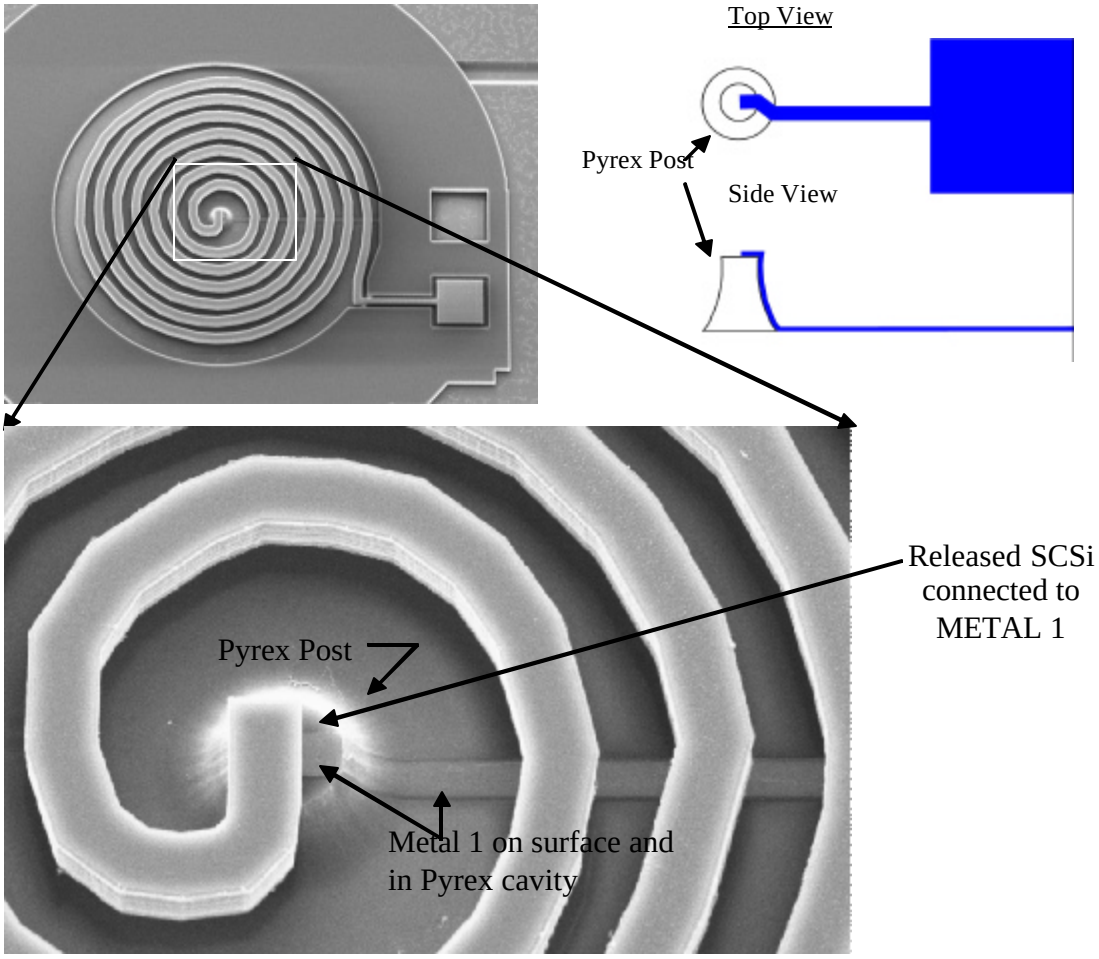


Figure 3-5 – Inductor example to show Metal 1 to Metal 2 connection through the silicon and Metal 1 on the surface of the Pyrex.

Below are two design examples to illustrate this rule:

1) *Example 1:* How can I access my electrodes of METAL1 layer inside my fully enclosed channel?

   -Have a 10µm wire trace come out of the channel and continue for at least 20µm, then have it recess into a 2µm cavity where it opens up into a bonding pad.

2) *Example 2:* How can a designer get access to the middle to build an inductor?

- Make a 20µm x 20µm post in the Pyrex etch. (Don't forget to account for the isotropic etch; It must be 1.2 times the depth wider than this in the mask layout.) Design a 10µm wire trace that starts on the post 10µm from one end and follows into the cavity where it will open up to a bonding pad. The centre of the inductor will then make connection to this wire trace. Open up the SCSi layer above the bonding pad so access is made. This is shown below in Figure 3-5.

3.7. Rule 7: SCSi (Single Crystal Silicon) Minimum Feature Size

The minimum feature size for the SCSi layer is to be no less than 2µm.

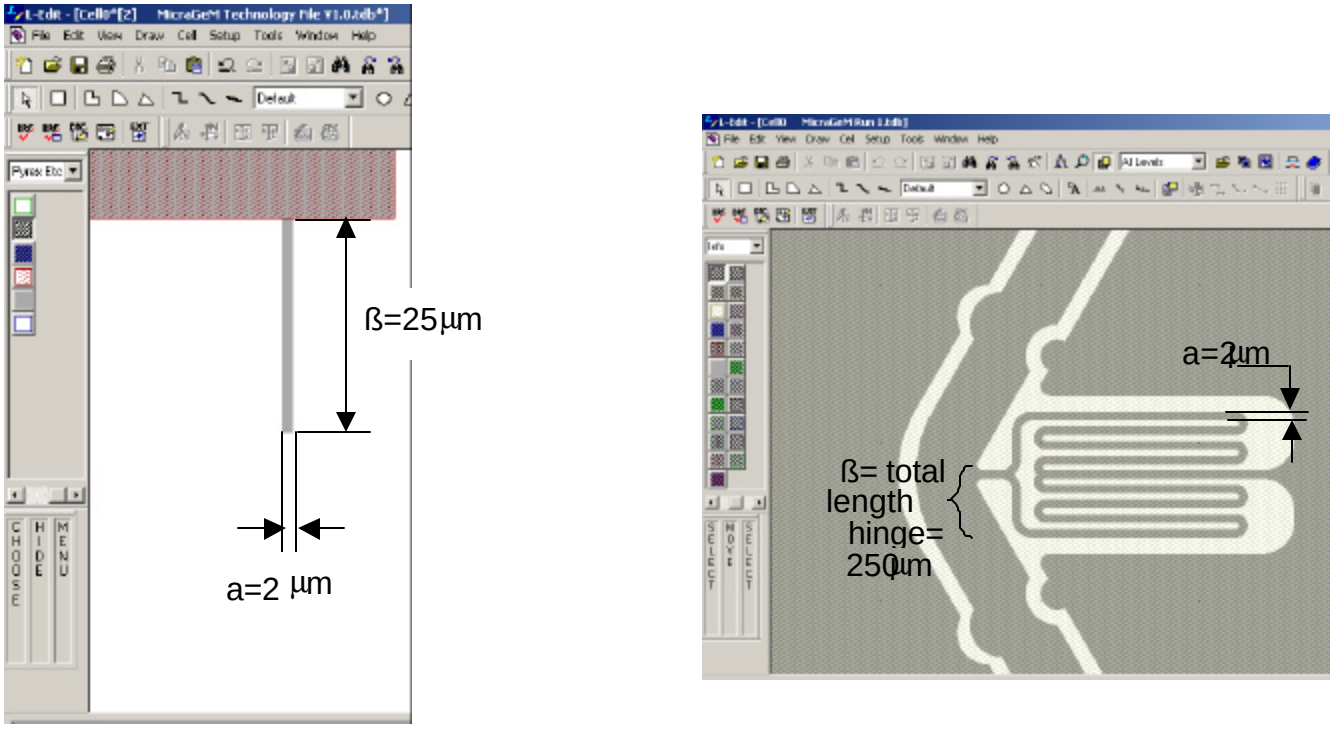
3.8. Rule 8: Maximum Feature Length

In the DRIE SCSi layer, the *maximum* ratio of a feature's width, *a*, to it's length, *ß*, is shown below in Equation 3-2:

$$MaximumFeatureRatio = \frac{a}{b} = \frac{1}{125} \qquad \text{(Equation 3-2)}$$

In the example, a minimum feature width of 2µm is being used to make a cantilever as shown in Figure 3-6(a). According to Equation 3-2, this cantilever is restricted to a maximum length of 250µm. The same equation can be used for features with changing direction, such as the serpentine hinge design shown in Figure 3-6(b) (estimate as close as possible).

This design rule has not been incorporated in the DRC file that is embedded in the Micragem technology file. Therefore, the design cannot automatically be checked for this rule and designers must verify it manually.



(a) **(b)**

Figure 3-6: (a) Maximum Aspect Ratio for a Cantilever Beam Figure
(b): Maximum Aspect Ratio for a Serpentine Hinge Design

3.9. Rule 9: METAL2 (on Silicon) Minimum Feature Size

The minimum feature size for the METAL2 (on Silicon) layer is 5µm.

3.10. Rule b10: METAL2 is Self Aligned to SCSi layer

METAL2 (on Silicon) must enclose the SCSi layer by at least 1.5 µm to ensure they are aligned. An example is shown below in Figure 3-7.

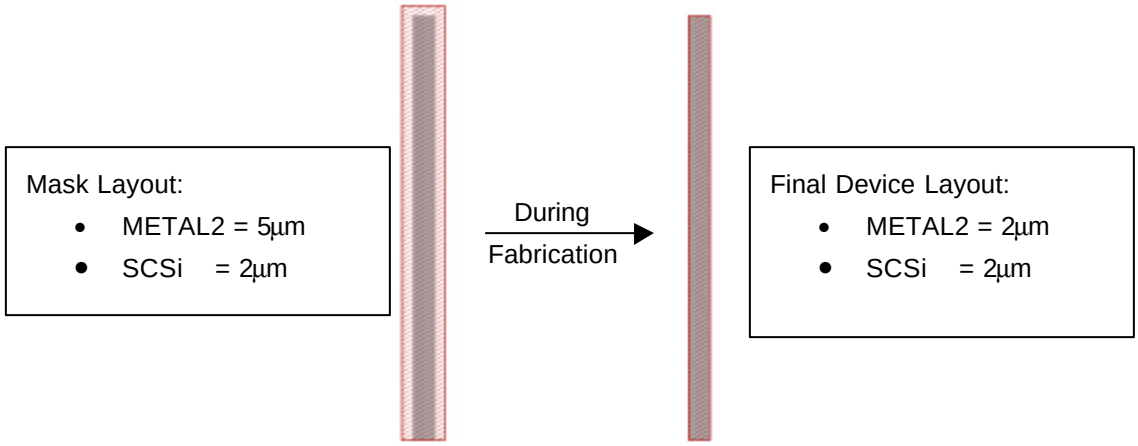


Figure 3-7: METAL2 Self Aligned to Released Silicon Features

This self-alignment ensures the top metal layer lines up exactly to the remaining silicon upon deep reactive ion etching. However, if METAL2 is drawn on silicon that is not being etched, the dimensions will not change during fabrication. This is shown below in Figure 3-8.

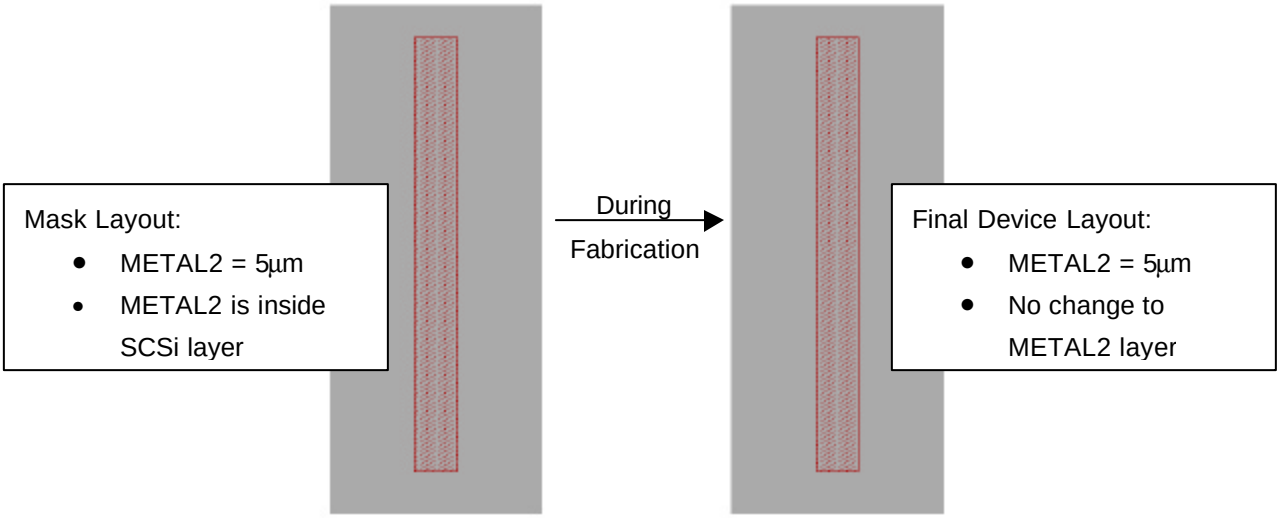


Figure 3-8: METAL2 is NOT Self-Aligned to SCSi Features Wider than METAL2 Feature

METAL2 appears on top of SCSi features only. So it is important that at least some part the METAL2 layer stays inside the SCSi layer. This is shown in Figure 3-9. Any METAL2 feature drawn outside the SCSi layer will be removed during processing and these features **will be lost**. For automatic design rule checking for this condition, make sure that the following option for design rule 10 is unchecked in the DRC setup file in the MEMSPro tool.

To access the DRC setup file:

1. In the **MEMSPro L-Edit Window**, select the following from the main menu: **TOOLS | DRC setup**
2. Un-check the checkbox for **if layer 1 completely outside layer 2**

When running DRC with this option, you can ignore the errors that appear for the types of features in figure 3-8.

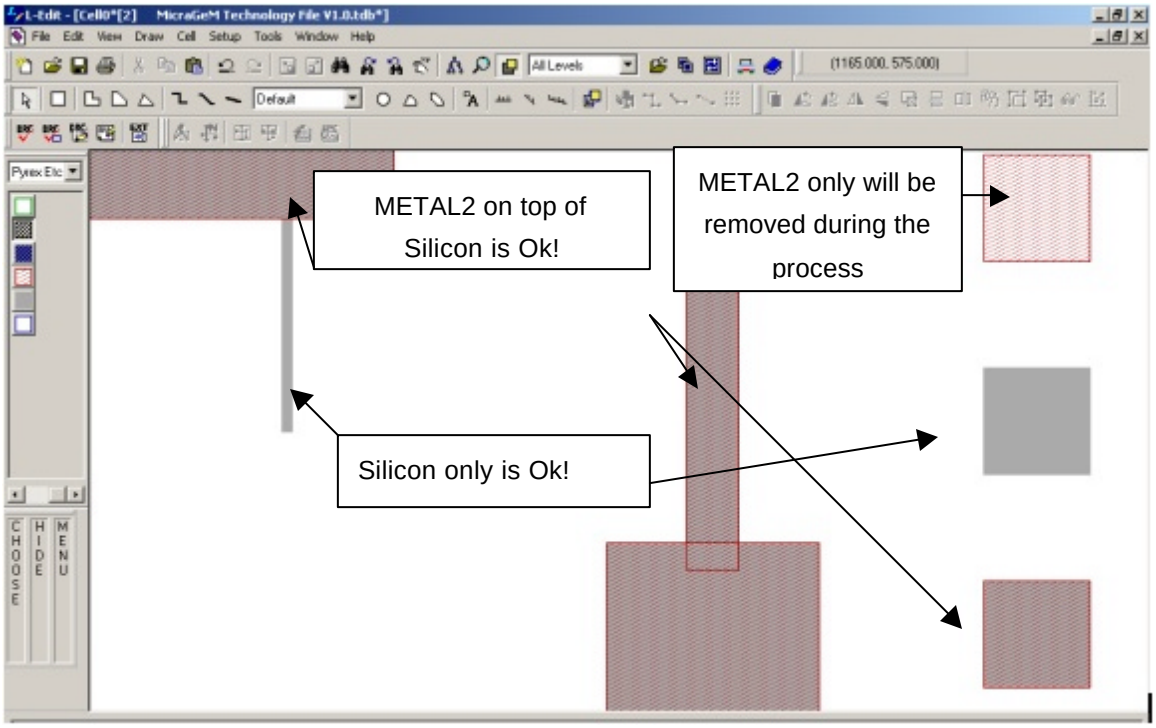


Figure 3-9: METAL2 Features Must Appear on Top of SCSi Layer

3.11. Rule 11: Minimum Spacing Between SCSi Layers

The minimum spacing between SCSi features is to be no less than 2µm.

3.12. Rule 12: No etched circles in Metal2 or SCSi Layers

The enclosed circles less than **50mm diameter** in the SCSi and Metal2 layers are not permissible. However, circle islands are ok. Designer should use Hole_SCSi and Hole_M2 layers to define holes in SCSi and METAL2 layers respectively. Further testing will be done to alleviate the problems associated with smaller features. The following figure illustrates this.

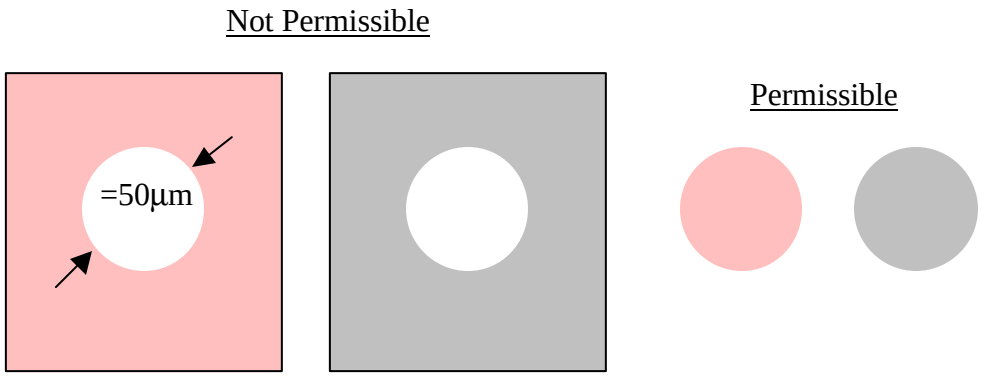


Figure 3-10: Etched circles less than 50mm not allowed in Metal 2 and SCSi Layers

Tables 3-1 and 3-2 summarize the design rules of the Micragem process for the given options.

	Min feature Size (µm)	Max feature Length (µm)	Pyrex Etch Depth (µm)	Min Trench Width (µm)	Thickness (µm)	Figure No.
PYREX Etch (Pyrex wafer)	5 or 10 (Rule2)		2, 10, or 12 (Rule 1)	9.8, 29 or 38.8 (Rule 2)	525	3-1 3-2
METAL1 (on Glass)	10 (Rule 4)				0.3	
SCSi (Rule 7)	2	250			10	3-6
METAL2 (On Silicon)	5 (Rule 9)				0.85 (nm)	

Table 3-1: Feature Size Rules of Layers

	Rule #	Figure No.	Min Value (μm)
Pyrex cavities must be linked by 5μm lines (except when a fully enclosed cavity is crucial i.e. microfluidic channels)	3	3-3	Width of linking lines = 5
METAL1 must lie within PYREX Etch (minimum distance from outside edge of PYREX Etch feature to METAL1 features)	5	3-4	Mask 1 = 2 Mask 2 = 0
METAL 1 on Surface of PYREX	6	3-5	
Minimum Spacing Between METAL1 Layers	5		12
METAL2 is self aligned to SCSi layer	10	3-7 3-8	1.5
No METAL2 outside SCSi	10	3-9	
Minimum Spacing between SCSi layers	11		2
No etched enclosed circles in the METAL2 and SCSi layers less than 50μm.	12	3-10	50

Table 3-2: General Rules

4 Material Properties

Table 4-1: Single Crystal Silicon Membrane

Thickness	10µm ± 2%
Resistivity (boron doped, p-type)	2.756 Ohm·cm
Elastic Modulus <100>	1.295 e^{11} N/m^2 [1]
Density	2320 kg/m^3 [2]
Dielectric Constant	13.5 [3]

Table 4-2: Metal 1

Sheet Resistance	TBA
Stress	TBA
Elastic Modulus*	6.13 x 10^{10} N/m^2 [3]
Density	19 300 kg/m^3 [4]

Table 4-3: Metal 2

Sheet Resistance	TBA
Stress	TBA
Elastic Modulus*	6.13 x 10^{10} N/m^2 [3]
Density	19 300 kg/m^3 [4]

* Value is for vacuum-evaporated polycrystalline film (300ºC). Micragem film is sputtered.

5 Wirebonding and Packaging

The packages offered are shown in Table 5-1 below:

9mm x 5mm chip	4mm x 5 mm chip
68 PGA	84 PGA
84 PGA	40 DIP

Table 5-1: Packages offered for Micragem

- 40 DIP is not offered for the bigger chip because it does not fit in the cavity.
- 68 PGA is not offered for the smaller chip because the wire is required to be over 8000µm long.

5.1. Requirements for Packaging

1) The minimum pad size is 100µm x 100µm and the minimum pitch is 150µm. That is, 100µm x 100µm square pad with 50µm space in between each pad. This is illustrated in Figure 5-1.

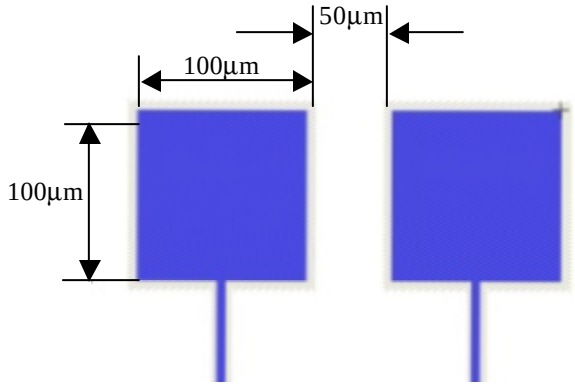


Figure 5-1: Minimum Bonding Pad size and Pitch

2) There are to be no more pads on one side than bonding fingers. This alleviates forcing a bond to the adjacent side as shown below in Figure 5-2.
3) All pads are to be aligned. This is illustrated in Figure 5-2.
4) Spread pads as much as possible. This is illustrated in Figure 5-2.

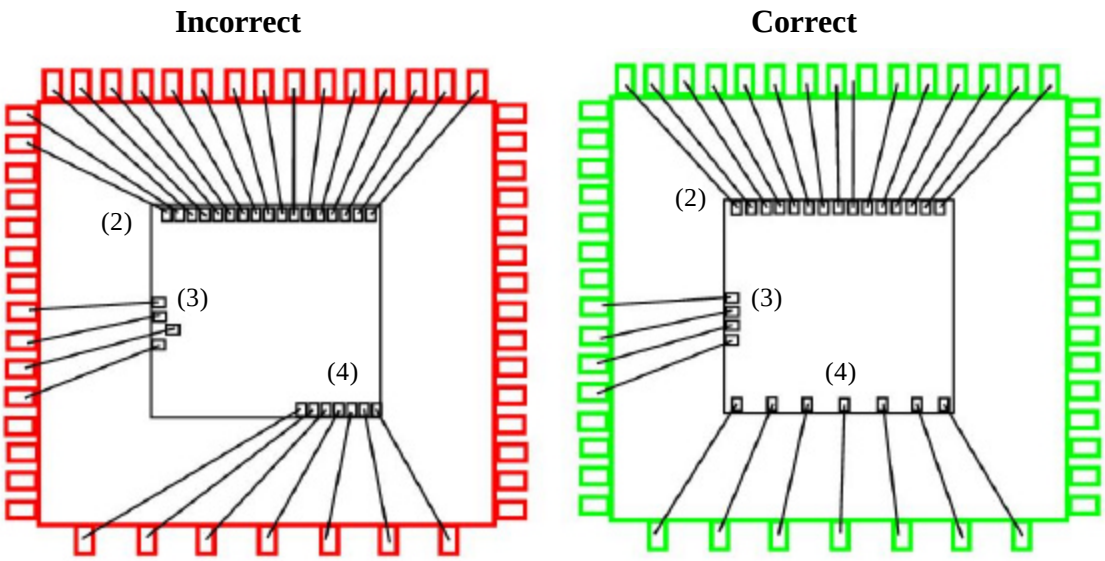
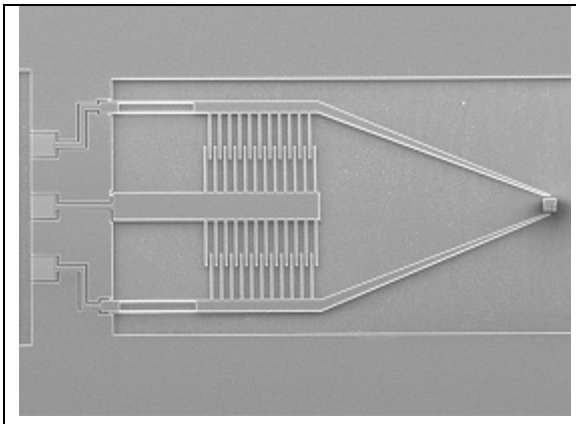


Figure 5-2: Bonding Requirements Illustrated

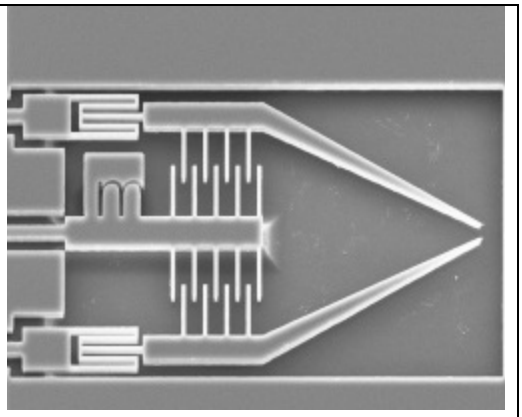
5) A bonding diagram must be completed for chips requiring bonding and included with the submitted design. Bonding diagrams are available from the CMC website.

6 Micragem Design Examples

Figures 4-1 to 4-4 show MEMS devices that were successfully fabricated by Micralyne's engineers.

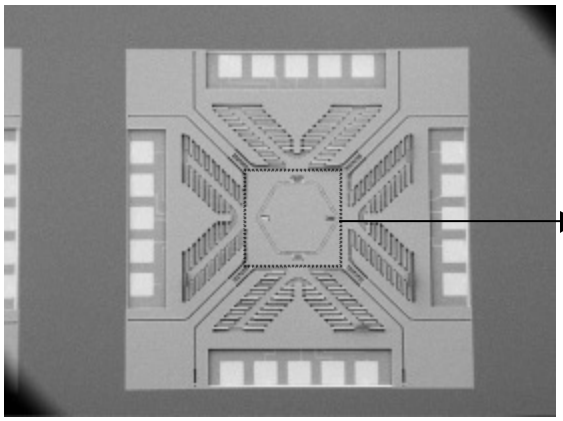


Example 1: Comb-Drive Actuated Micro Tweezers

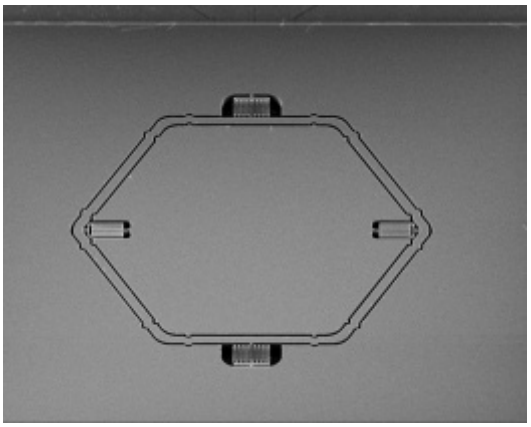


Example 2: Comb-Drive Actuated Micro Tweezers

Figure 6-1: Comb-Drive Actuated Micro Tweezers

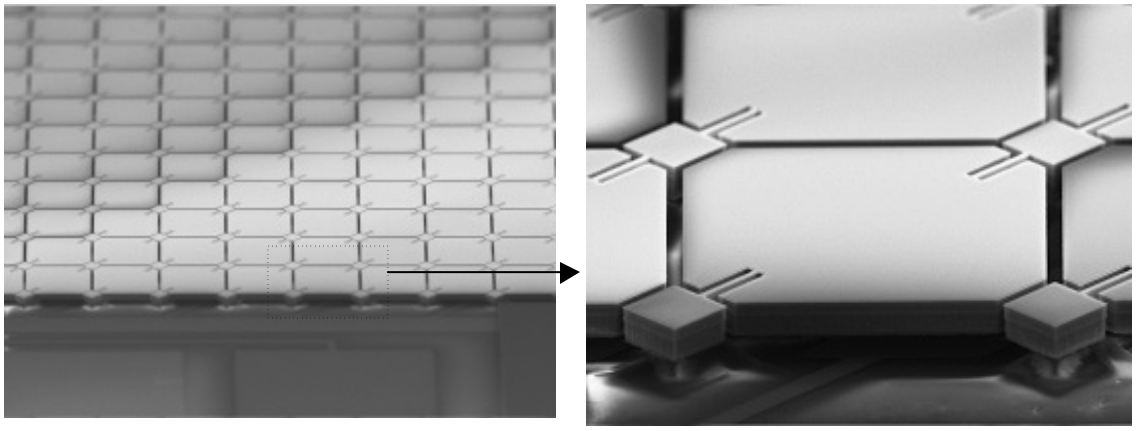


Example 3: Optical MEMS - 3D Optical Mirror



Close-up of Mirror

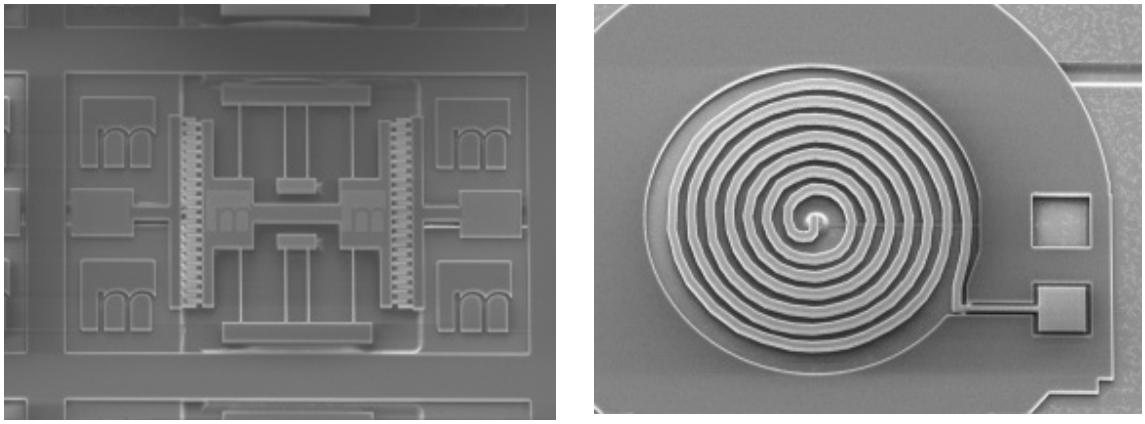
Figure 6-2: 3D Optical Mirrors



Example 4: Optical MEMS - Digital Mirror Array

Close-up of Mirror

Figure 6-3: Digital Mirror Array



Example 5: RF MEMS - Resonator

Example 6: RF MEMS - Inductor

Figure 6-4: Resonator and Inductor

2) References

[1] J. C. Greenwood, "Silicon in Mechanical Sensors," *Journal of Physics E, Scientific Instrumentation*, vol. 21, pp. 1114-1128, 1988.

[2] M. J. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization*, 2nd ed. USA: CRC Press LLC, 2002.

[3] H. Santos, *Introduction to Microelectromechanical (MEM) Microwave Systems.* Norwood, MA: Artech House, 1999.

[4] Internet, "www.webelements.com," 2004.

General Reference:

T. Zhou, P. Wright, J. Crawford, G. McKinnon, Y. Zhang, "MEMS 3D Optical Mirror/Scanner" The 2003 international Conference on MEMS, NANO and Smart Systems, 20-23 July, 2003, Banff, Canada, pp: 222-226.